# CSO 2130 Instruction Set Architecture

Daniel G. Graham PhD



**ENGINEERING** 

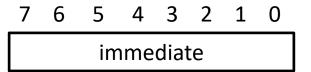
# **REVIEW**



# SUBSET OF OUR TOY ISA

icode	b	Behavior
0		rA=rB
1		rA+=rB
2		rA&=rB
6	0	rA=read from memory at pc + 1 Also written as rA = M[pc+1]

7	6	5	4	3	2	1	0	
R	i	cod	e	,	a		b	1







- 1. Full overview of Toy ISA
- Some memory Operations with the Toy ISA
- 3. Loops and Conditionals with Toy ISA
- Writing and simulating more complex programs with Toy ISA

icode	b	meaning	
0		rA = rB	<b>FULL ISA</b>
1		rA += rB	I OLL 15/1
2		rA &= rB	
3		<b>rA</b> = read from memory at address <b>rB</b>	We'll give
4		write <b>rA</b> to memory at address <b>rB</b>	full descr
5	0	rA = ~rA	of ISA at
	1	rA = -rA	
	2	rA = !rA	begin of
	3	rA = pc	exam. In
6	0	rA = read from memory at pc + 1	— a picture
	1	rA += read from memory at pc + 1	we will g
	2	$\mathbf{rA}$ &= read from memory at $\mathbf{pc}$ + $1$	
	3	$\mathbf{rA}$ = read from memory at the address stored at $\mathbf{pc}$ + 3	1
		For icode 6, increase <b>pc</b> by 2 at end of instruction	
7		Compare <b>rA</b> as 8-bit 2's-complement to <b>0</b>	
		if rA <= 0 set pc = rB	
		else increment <b>pc</b> as normal	UNIVERSITY EN

We'll give the full description of ISA at the begin of every exam. In fact this a picture of what we will give you.



	icode	b	meaning	
	0		rA = rB	<b>FULL ISA</b>
	1		rA += rB	I OLL 15/1
	2		rA &= rB	
	3		<b>rA</b> = read from memory at address <b>rB</b>	More op
	4		write <b>rA</b> to memory at address <b>rB</b>	with imm
_	5	0	rA = ~rA	— Wich iiiiii
		1	rA = -rA	
		2	rA = !rA	
		3	rA = pc	
	6	0	rA = read from memory at pc + 1	
		1	rA += read from memory at pc + 1	
		2	rA &= read from memory at pc + 1	
		3	rA = read from memory at the address stored at $pc$ + 1	
			For icode 6, increase <b>pc</b> by 2 at end of instruction	
	7		Compare <b>rA</b> as 8-bit 2's-complement to <b>0</b>	
			if rA <= 0 set pc = rB	I Is you can be a second
			else increment <b>pc</b> as normal	VIRGINIA

More operations with immediates



# **MEMORY OPERATIONS**

icode	b	mea	ıning														
0		rA	= rE	3													
1		rA	+= r	'B													
2		rA	&= r	'B													
3		rA:	read from memory at address rB  e rA to memory at address rB  tricky. So, let's spend some														
4		writ	e <b>rA</b>	to i	memory	at addı	ress <b>rB</b>				tricl	cy. S	50, l	et's	spe	nd som	ıe
											time	e or	the	em.			
7 6	5 5	4	3	2	1 0			7	6	5	4	3	2	1	0	_	
R	ico	de	a		b					in	nme	dia	te				

# READ FROM MEMORY ADDRESS STORED IN RB

Registers

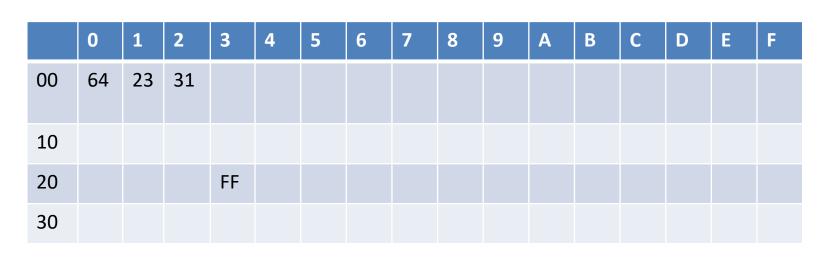
RO X

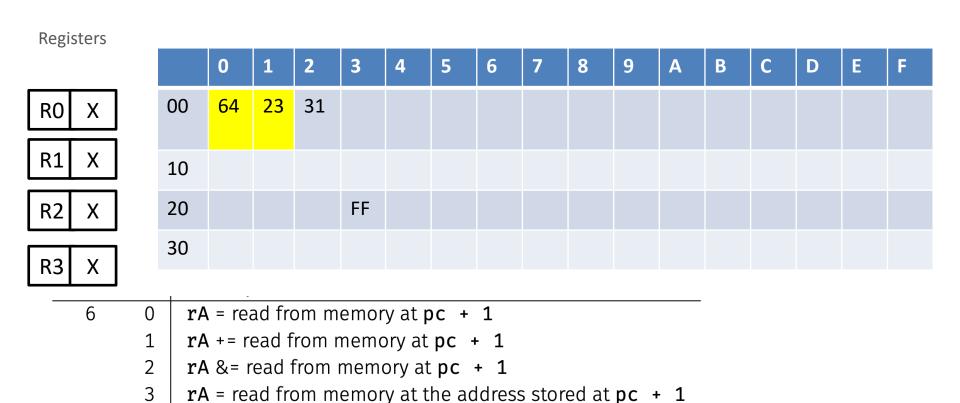
R1 X

R2 X

R3 X

PC 00





For icode 6, increase **pc** by 2 at end of instruction

RO X

R1 X

R2 X

R3 X

PC 00

	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	Е	F
00	64	23	31													
10																
20				FF												
30																

6 0 rA = read from memory at pc + 1

7 6 5 4 3 2 1 0 R icode a b 7 6 5 4 3 2 1 0 immediate

RO X

R1 X

R2 X

R3 X

PC 00

	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	Е	F
00	64	23	31													
10																
20				FF												
30																

6 0 rA = read from memory at pc + 1

 7
 6
 5
 4
 3
 2
 1
 0

 0
 1
 1
 0
 0

7 6 5 4 3 2 1 0



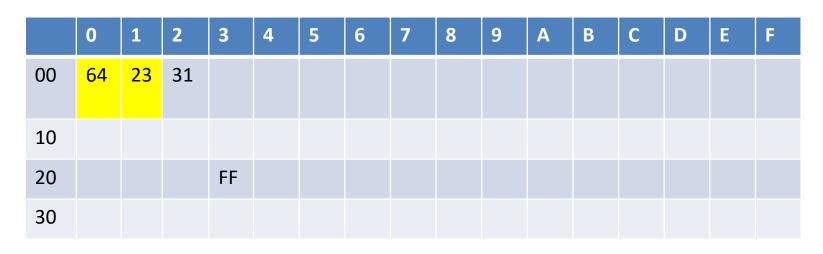


R1 23

R2 X

R3 X

PC 02



PC Updates to 2 so what instruction will we execute next?





R1 23

R2 X

R3 X

PC 02

	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	Е	F
00	64	23	31													
10																
20				FF												
30																

icode	b	meaning
0		rA = rB
1		rA += rB
2		rA &= rB
3		<b>rA</b> = read from memory at address <b>rB</b>
4		write ${f r}{f A}$ to memory at address ${f r}{f B}$

RO X

R1 23

R2 X

R3 X

PC 02

	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	Е	F
00	64	23	31													
10																
20				FF												
30																

3  $\mathbf{r}\mathbf{A}$  = read from memory at address  $\mathbf{r}\mathbf{B}$ 

7 6 5 4 3 2 1 0 R icode a b 7 6 5 4 3 2 1 0 immediate

RO X

R1 23

R2 X

R3 X

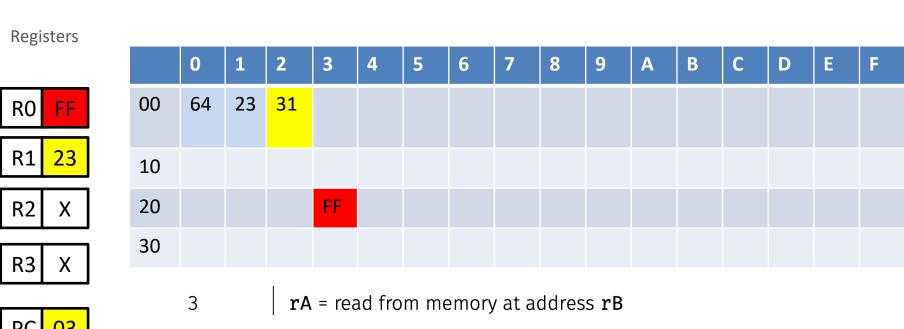
PC 02

	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	E	F
00	64	23	31													
10																
20				FF												
30																

3  $\mathbf{r}\mathbf{A}$  = read from memory at address  $\mathbf{r}\mathbf{B}$ 

 7
 6
 5
 4
 3
 2
 1
 0

 0
 0
 1
 0
 0
 0



7 6 5 4 3 2 1 0 0 011 00 01

RB is R1 and it stores 0x23. So, we go location 23 in memory and retrieve the value 0xFF.

STOP. And talk to you neighbor



icode	b	meaning
0		rA = rB
1		rA += rB
2		rA &= rB
3		rA = read from memory at address rB
4		write <b>rA</b> to memory at address <b>rB</b>
5	0	rA = ~rA
	1	rA = -rA
	2	rA = !rA
	3	rA = pc
6	0	rA = read from memory at pc + 1
	1	rA += read from memory at pc + 1
	2	rA &= read from memory at pc + 1
	3	rA = read from memory at the address stored at pc + 1
		For icode 6, increase <b>pc</b> by 2 at end of instruction
7		Compare <b>rA</b> as 8-bit 2's-complement to <b>0</b>
		if rA <= 0 set pc = rB
		else increment <b>pc</b> as normal

Let's look at this instruction now?



# READ FROM MEMORY ADDRESS STORED IN RB

Registers

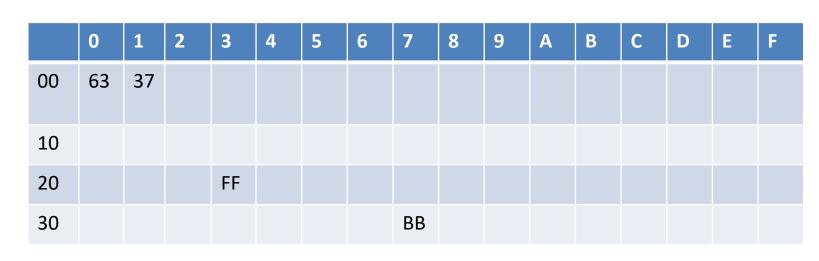
RO X

R1 X

R2 X

R3 X

PC 00



R0	Χ
----	---

R1 X

R2 X

R3 X

PC 00

	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	Е	F
00	63	37														
10																
20				FF												
30								ВВ								

_	6	0	rA = read from memory at pc + 1
		1	rA += read from memory at pc + 1
		2	rA &= read from memory at pc + 1
		3	rA = read from memory at the address stored at pc + 1
			For icode 6, increase <b>pc</b> by 2 at end of instruction

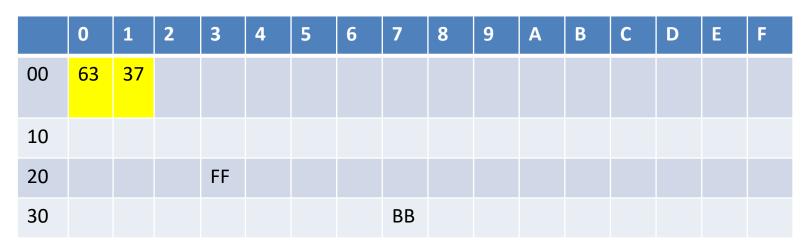
RO X

R1 X

R2 X

R3 X

PC 00



rA = read from memory at the address stored at pc + 1For icode 6, increase pc by 2 at end of instruction

7 6 5 4 3 2 1 0 R icode a b 7 6 5 4 3 2 1 0 immediate

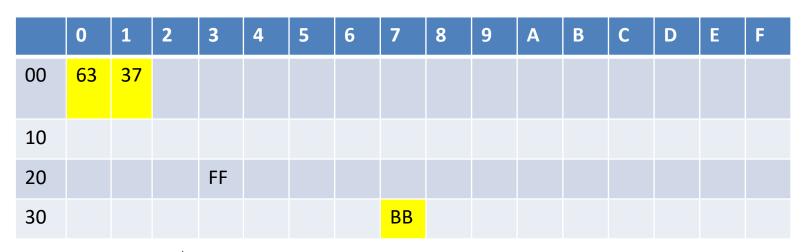
RO BB

R1 X

R2 X

R3 X

PC 00



3 **rA** = read from memory at the address stored at **pc** + **1**For icode 6, increase **pc** by 2 at end of instruction

 7
 6
 5
 4
 3
 2
 1
 0

 0
 1
 1
 0
 0
 1
 1

7 6 5 4 3 2 1 0

# MEMORY WRITES WORK IN A SIMILAR WAY



### **REGISTER SPILLING**

Because we have a limited number of registers, we can't store all variables in registers, so we must store some in memory and read them into a register when we need them. Here is the strategy

- Read the register value to a predetermined location in memory.
- Use the register
- Write the register value back to memory, so that it can be used to store something else

Architecture	8 bit	32 bit	64 bit
ARM	X	15	31
Intel x86	X	8	16
Toy ISA	4	X	Х

# **REGISTER SPILLING**

$$R0 = M[0x31]$$
  
 $R0 += 2$   
 $R1 = 0x31$   
 $M[R1] = R0$ 

After this point R0 can be used for something else

# **REGISTER SPILLING**

R0 =	M[(	)x31	]
R0 +:	= 2		
R1 =	0x3	31	
M[R1	] =	R0	

icode	b	meaning
0		rA = rB
1		rA += rB
2		rA &= rB
3		rA = read from memory at address rB
4		write <b>rA</b> to memory at address <b>rB</b>

$$M[RB] = RA$$

$$R0 = M[0x31]$$
 0x63 0x31

$$R0 += 2$$
 0x61 0x02

$$R1 = 0x31$$
 **0x64 0x31**

$$M[R1] = R0 0x41$$

			0	1	2	3	4	5	6	7	8	9	Α	В	С	D	E	F
R0	X	00	63	31	61	02	64	31	41									
R1	Χ																	
R2	Х	10																
112		20																
R3	Χ	30		02														

PC 00

$$R0 = M[0x31]$$
 0x63 0x31

$$R0 += 2$$
 0x61 0x02

$$R1 = 0x31$$
 **0x64 0x31**

$$M[R1] = R0 0x41$$

R0

R1

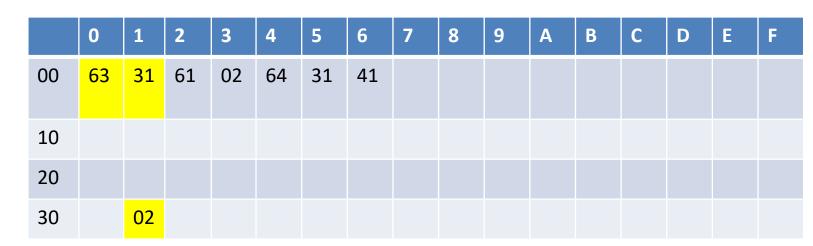
R2

R3

02

X

Χ



PC 00

$$R0 = M[0x31]$$
 0x63 0x31

$$R0 += 2$$
 0x61 0x02

$$R1 = 0x31$$
 **0x64 0x31**

$$M[R1] = R0 0x41$$

20		0	1	2	3	4	5	6	7	8	9	Α	В	С	D	Е	F
R0 04	00	63	31	61	02	64	31	41									
R1 X																	
R2 X	10																
NZ A	20																
R3 X	30		02														

PC 02

$$R0 = M[0x31]$$
 0x63 0x31

$$R0 += 2$$
 **0x61 0x02**

$$R1 = 0 \times 31 \qquad 0 \times 64 \times 0 \times 31$$

$$M[R1] = R0 0x41$$

02

#### Registers

			0	1	2	3	4	5	6	7	8	9	Α	В	С	D	E	F
R0	04	00	63	31	61	02	64	31	41									
R1	31																	
		10																
R2	Х	20																

PC 04

30

R3

$$R0 = M[0x31]$$
 0x63 0x31

$$R0 += 2$$
 0x61 0x02

$$R1 = 0x31$$
 0x64 0x31

$$M[R1] = R0 0x41$$

R0

R1

R2

R3

04

31

	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	Е	F
00	63	31	61	02	64	31	41									
10																
20																
30		04														

PC 06

# **CONDITIONAL IF ELSE**

$$x = M[0x0F]$$

If  $x > 0$ :

 $x += 1$ 

Else:

 $x &= 7$ 

Memory Map IO (Input/output)

Let's implement this program using our instructions

		1	
icode	b	meaning	
0		rA = rB	
1		rA += rB	
2		rA &= rB	
3		$\mathbf{r}\mathbf{A}$ = read from memory at address $\mathbf{r}\mathbf{B}$	
4		write ${f r}{f A}$ to memory at address ${f r}{f B}$	
5	0	rA = ~rA	
	1	rA = -rA	
	2	rA = !rA	
	3	rA = pc	
6	0	rA = read from memory at pc + 1	
	1	rA += read from memory at pc + 1	
	2	rA &= read from memory at pc + 1	
	3	$\mathbf{r}\mathbf{A}$ = read from memory at the address stored a	at <b>pc + 1</b>
		For icode 6. increase pc by 2 at end of instrucți	on
7		Compare <b>rA</b> as 8-bit 2's-complement to <b>0</b>	
		if <b>rA &lt;= 0</b> set <b>pc = rB</b>	
		else increment <b>pc</b> as normal	





# LET'S ALLOCATE REGISTERS AND PICK INSTRUCTIONS

x & &= 7

# LET'S CALCULATE WHERE TO JUMP TO

#### **Memory Address**

0x00

#### R0 = M[0x20]

0x02 R1 =

0x04 If R0 <= 0 set PC= R1

0x05 R0 += 1

0x07 R0 &= 2

#### Size of Instruction

2 Bytes

2 Bytes

1 Byte

2 Bytes

2 Bytes

So what address do we want R1 to be?

# LET'S CALCULATE WHERE TO JUMP TO

#### **Memory Address**

# 0x00 R0 = M[0x20] 0x02 R1 = 0x07 0x04 If R0 <= 0 set PC= R1 0x05 R0 += 1 0x07 R0 &= 2

So what address do we want R1 to be?

#### Size of Instruction

- 2 Bytes
- 2 Bytes
- 1 Byte
- 2 Bytes
- 2 Bytes

# LET'S CALCULATE WHERE TO JUMP TO

#### **Memory Address**

x &= 7



0x02

0x04

0x05

0x07

$$R0 = M[0x20]$$

$$R1 = 0x07$$

If 
$$R0 \ll 0$$
 set  $PC = R1$ 

$$R0 += 1$$

$$R0 \&= 2$$

So what address do we want R1 to be?

Be really careful of the fall through case.

# **LOOPS**



icode	b	meaning
0		rA = rB
1		rA += rB
2		rA &= rB
3		<b>rA</b> = read from memory at address <b>rB</b>
4		write <b>rA</b> to memory at address <b>rB</b>
5	0	rA = ~rA
	1	rA = -rA
	2	rA = !rA
	3	rA = pc
6	0	rA = read from memory at pc + 1
	1	rA += read from memory at pc + 1
	2	rA &= read from memory at pc + 1
	3	rA = read from memory at the address stored at $pc + 1$
		For icode 6, increase <b>pc</b> by 2 at end of instruction
7		Compare <b>rA</b> as 8-bit 2's-complement to <b>0</b>
		if <b>rA &lt;= 0</b> set <b>pc = rB</b>
		else increment <b>pc</b> as normal



First, rewrite as a do-while loop. (This due to limitation in Toy ISA) reasons will be clear

later.

```
x = 2

for (i = 0; i < 5; i++) {

x+=1

}
```

```
x = 2
i = 0
do{
    x+=1
    i++
} while (i<5)</pre>
```

```
x = 2
i = 0
do{}
x+=1
i++
} while (i<5)
```

$$R0 = 2$$

```
x = 2
i = 0
do{
    x+=1
    i++
} while(i<5)</pre>
```

$$R0 = 2$$

$$R1 = 0$$

```
x = 2
i = 0
do{
    x+=1
    i++
} while (i<5)</pre>
```

$$R0 = 2$$
  
 $R1 = 0$   
 $R2 = PC$ 

Store the memory address of the beginning of the loop

```
x = 2
i = 0
do{
    x+=1
    i++
} while(i<5)</pre>
```

```
R0 = 2
R1 = 0
R2 = PC
R0 += 1
```

```
x = 2
i = 0
do{}
x+=1
i++
} while (i<5)
```

```
x = 2
i = 0
do{
    x+=1
    i++
} while(i<5)</pre>
```

```
R0 = 2

R1 = 0

R2 = PC

R0 += 1

R1 += 1

R3 = R1

R3+= -5

if R3 <=0 then PC = R2
```

But wait is that correct?

# SEE IF YOU CAN ENCODE THIS AND RUN IT IN THE SIMULATOR



```
x = 2
i = 0
do{
    x+=1
    i++
} while(i<5)</pre>
```

```
R0 = 2

R1 = 0

R2 = PC

R0 += 1

R1 += 1

R3 = R1

R3+= -5

if R3 <=0 then PC = R2
```

But wait is that correct? Translating the condition can be tricky



```
x = 2
i = 0
do{
    x+=1
    i++
} while (i<5)</pre>
```

-3, -2, -1, 0, 1 (five times)

R0 = 2	0x60 02	
R1 = 0	0x64 0x00	
R2 = PC	0x5B	
R0 += 1	0x61 0x01	
R1 += 1	0x65 0x01	
R3 = R1	0x0D	
R3+=-4	0x6D 0xFC	
if R3 <=0	then $PC = R2$	0x7E

#### **Toy ISA Simulator**

Execute one instruction

Run with 1.5

seconds between instructions

Reset

# FROM TOY ISA TO RISC-V



### SOME PERPECTIVE (RISC-V)

# The RISC-V Instruction Set Manual Volume I: User-Level ISA

Document Version 2.2

Editors: Andrew Waterman<sup>1</sup>, Krste Asanović<sup>1,2</sup>

<sup>1</sup>SiFive Inc.,

<sup>2</sup>CS Division, EECS Department, University of California, Berkeley andrew@sifive.com, krste@berkeley.edu

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Available at: <a href="https://riscv.org/wp-content/uploads/2017/05/riscv-spec-v2.2.pdf">https://riscv.org/wp-content/uploads/2017/05/riscv-spec-v2.2.pdf</a>

31	25	24	20 19		15 14	12	11	7 6	0	
funct'	7	rs2	r	$\overline{\mathrm{s1}}$	func	t3	$\operatorname{rd}$	opcode		R-type
			•							•
imm[11:0]			r	s1	func	t3	$\operatorname{rd}$	opcode		I-type
			•		•					•
imm[11]	:5]	rs2	r	s1	func	t3	imm[4:0]	opcode		S-type
			•		•					•
imm[31:12]							$\operatorname{rd}$	opcode		U-type

R-Format: instructions using 3 register inputs

I-Format: instructions with immediates, loads

**S-Format:** store instruction

**U-Format:** instructions with upper immediates

Detailed Data Sheet: <a href="https://www.elsevier.com/">https://www.elsevier.com/</a> data/assets/pdf file/0011/297533/RISC-V-Reference-Data.pdf



## RISC VS CISC

RISC-V ADD

https://msyksphinz-self.github.io/riscvisadoc/html/rvi.html#addi X86 Add

https://www.felixcloutier.com/x86/add

