

COMPUTER SYSTEMS AND ORGANIZATION

Clocks and Flip-Flops

Daniel Graham



ENGINEERING

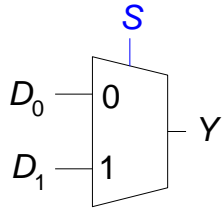


Contents

1. Muxes
2. Clocks
3. Flip Flops

MUXES

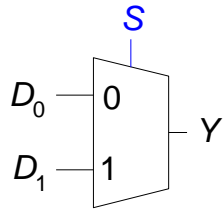
Example: 2:1 Mux



S	D_1	D_0	Y	S	Y
0	0	0	0	0	D_0
0	0	1	1	1	D_1
0	1	0	0		
0	1	1	1		
1	0	0	0		
1	0	1	0		
1	1	0	1		
1	1	1	1		

- Selects between one of N inputs to connect to output
- **Select** input is $\log_2 N$ bits – control input

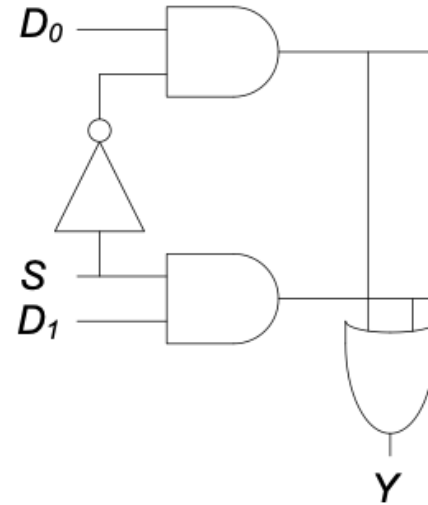
1 BIT MUX



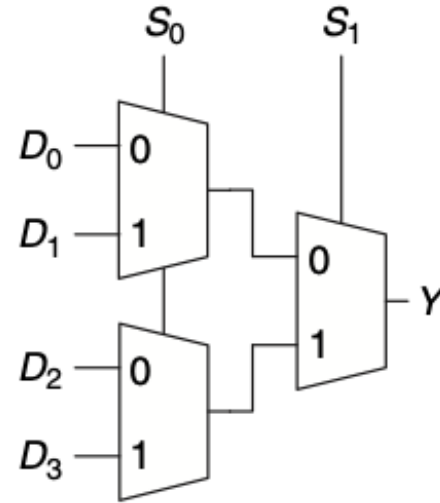
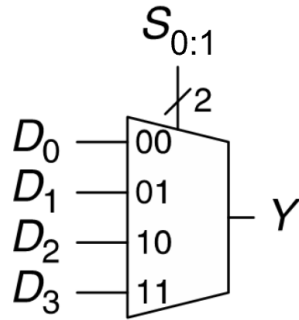
$$Y = D_0\bar{S} + D_1S$$

S	D ₁	D ₀	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

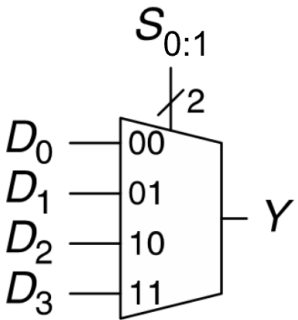
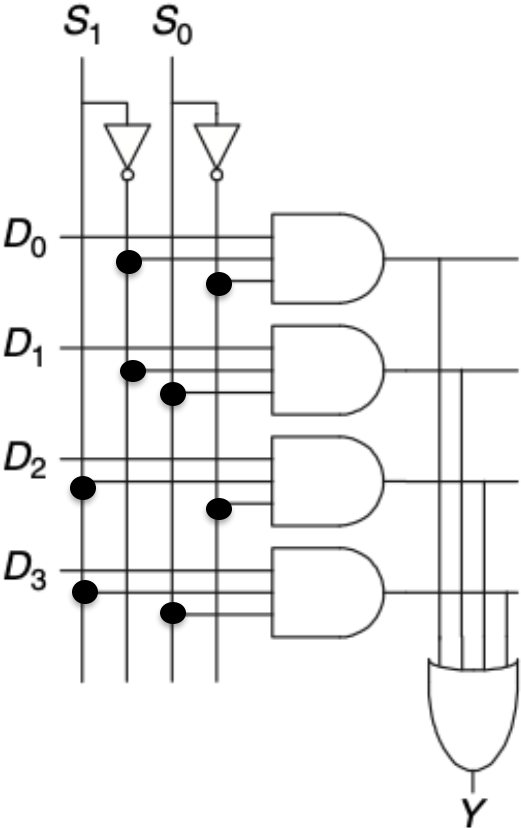
S	Y
0	D ₀
1	D ₁



2 BIT MUX



2 BIT MUX

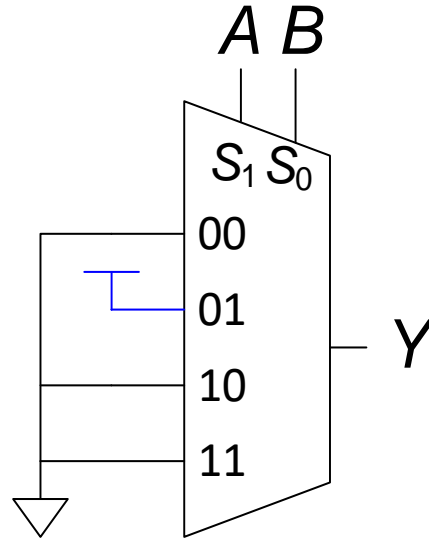


MUX AS A LOOK UP TABLE

Using mux as a **lookup table**

A	B	Y
0	0	0
0	1	1
1	0	0
1	1	0

$$Y = AB$$

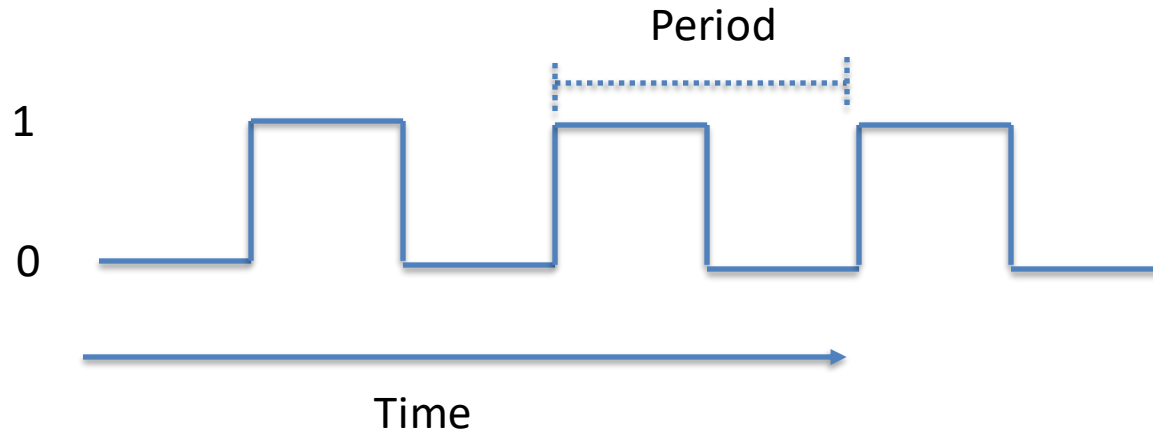


CLOCKS

A clock is something that produces a periodic signal

Period is length of time for one clock cycle

Example

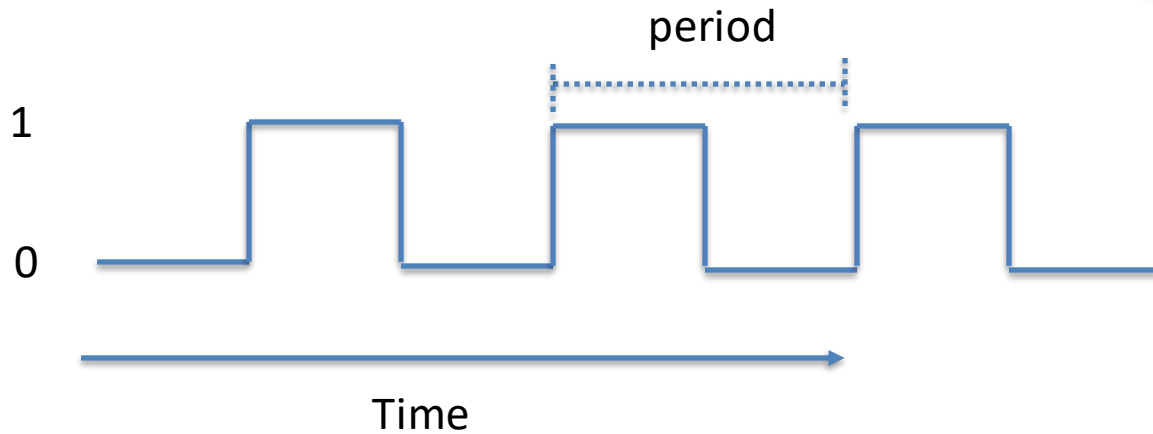


CLOCKS

Clock frequency Intel Core i-9 3.0GHz

Frequency = $1 / \text{period}$

Period = $1 / \text{frequency}$

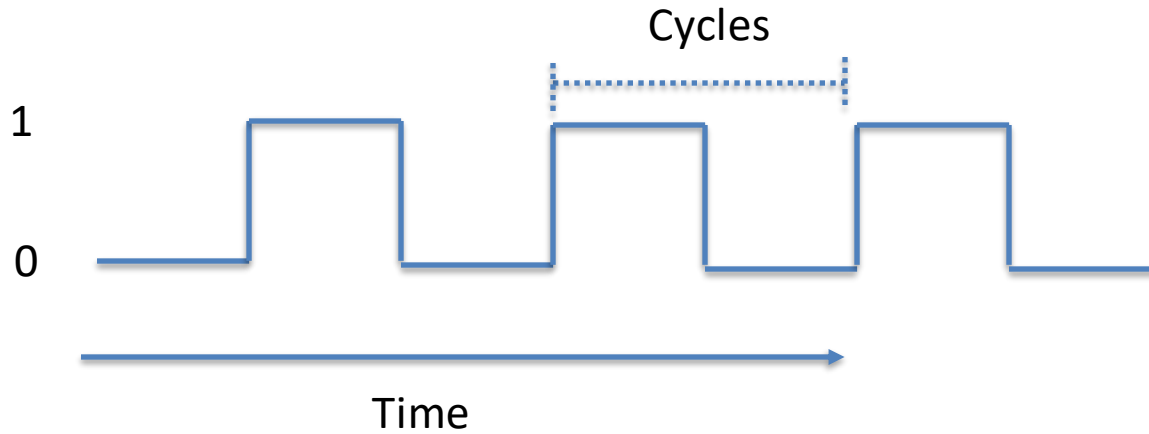


CLOCKS

Clock frequency Intel Core i-9

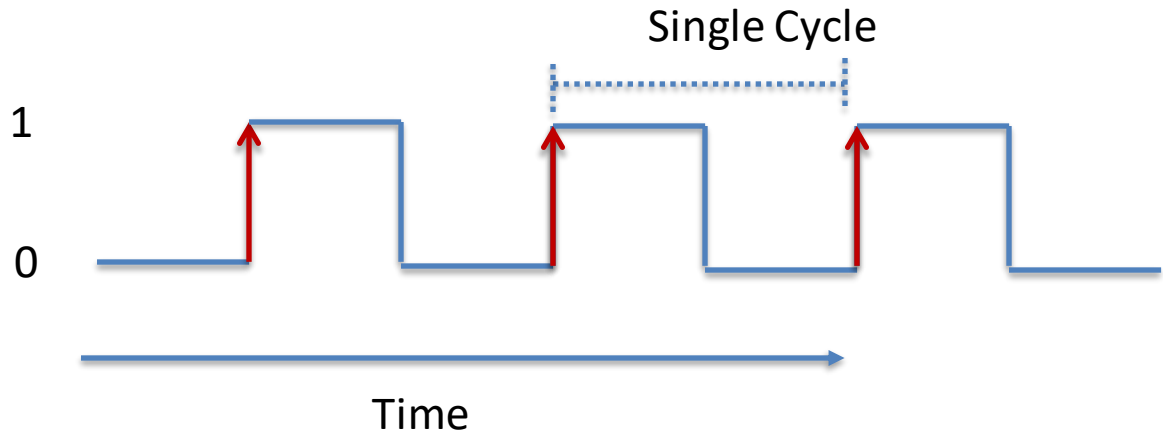
3.0GHz. = $3 * 10^9 = 3,000,000,000$ cycles per second

That is fast.



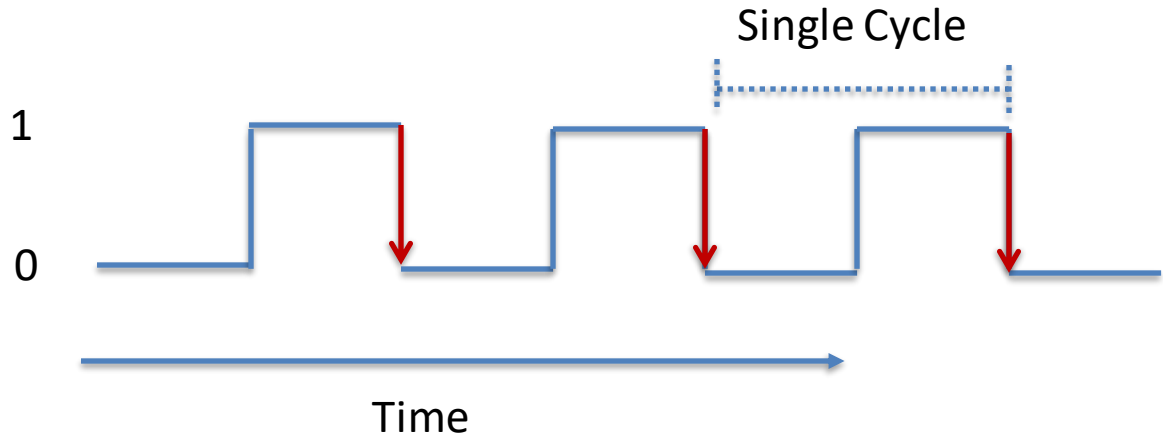
CLOCK EDGES

Rising Edge (Also called positive edge)



CLOCK EDGES

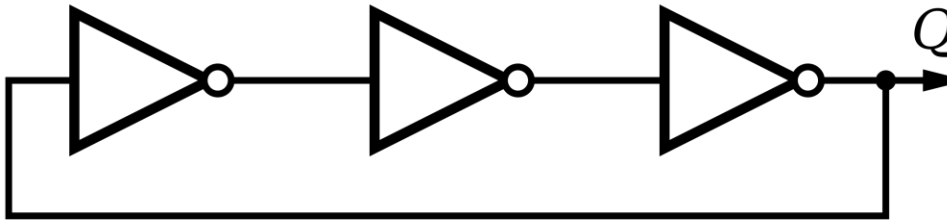
Falling Edge.



We will build a single cycle machine. It will complete all the computation in a single cycle

USING RING OSCILLATORS TO GENERATE CLOCKS

A clock is something that produces a periodic signal



Let's walk through an example and assume that Q starts off as 0. Draw the wave form that results.

$$\text{Frequency} = 1/(2*t*n)$$

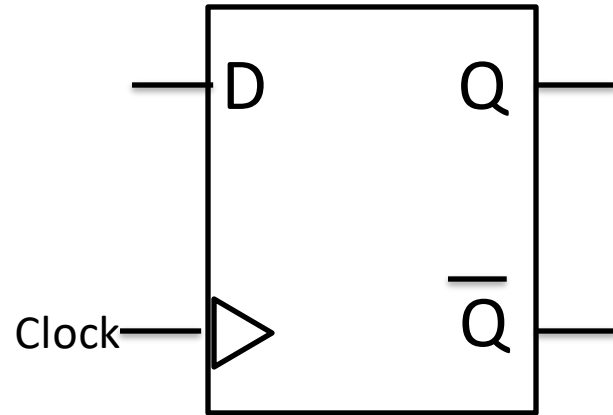
Where t is the time delay of an inverter and n is number of inverters

THE D FLIP FLOP

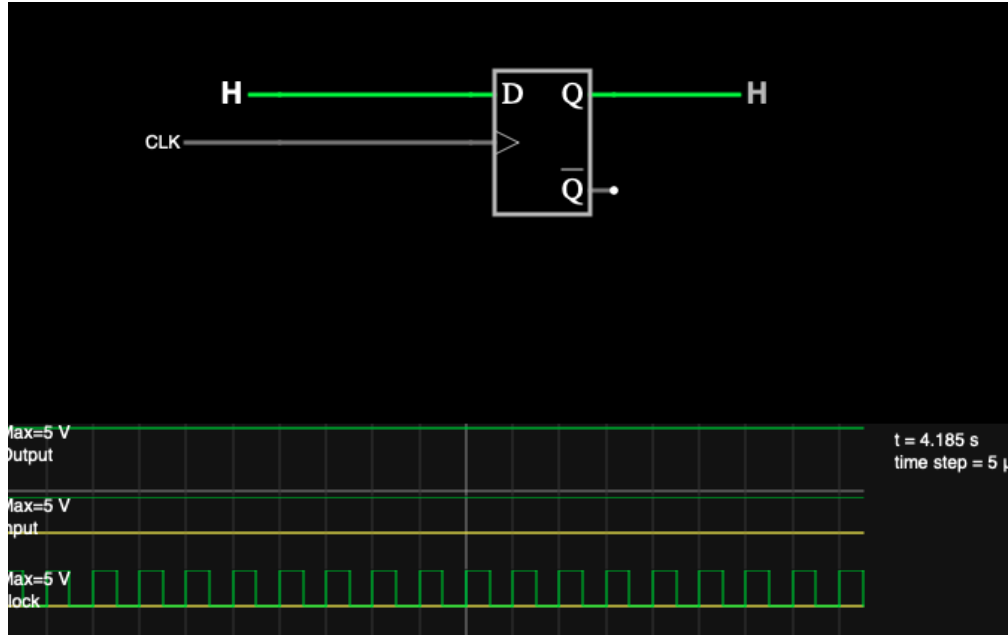
STORING SINGLE BITS

Goal

1. Understand the behavior of a positive edge-triggered D flip-flop.
 - How do we store a bit
 - What happens when the clock changes
 - What does it mean to be a positive edge triggered flip flop
 - What is Q and \overline{Q}



BUILT SIMULATOR VERSION



Use this link to experiment with the flipflop during lecture. Try different things and see how it works

<https://tinyurl.com/2dhk5kvq>

<http://www.falstad.com/circuit/circuitjs.html?ctz=CQAgjCAMB0I3BWcMBMcUHYMGZIA4UA2ATmIxAUgoqoQFMBaMMAKDASUPxABZsUQGPD178oFFgHcQXPKIE88VPgMhSZ3HoRGLI2qCwAyyJfN6KzVCADMAhgBsAznWpqASib064vfRAFGPijQSMFIVDAILACygpA6YkrKYIRhLAD21PrKkKSu0BBWIADyAK4ALgAOFrNgMil5eeGw8GSECIQo4SABINggAJYAdtXltQLZvLnE+fC5GO2d3QIC-QDG9ulrANYsQA>

D FLIP FLOP

Two inputs and Two outputs

Inputs

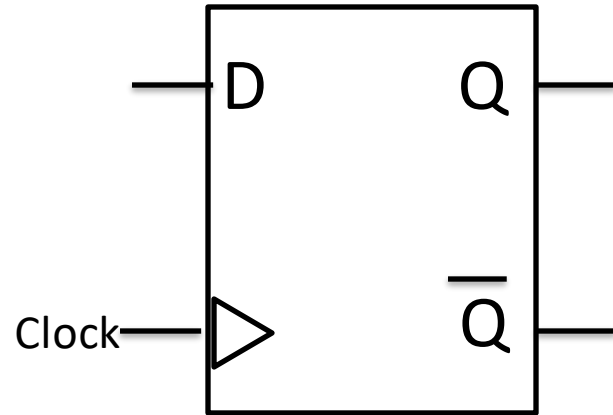
D – Data in (The single bit that we want the flip flop to store)

Clock – the output wave from the clocks we discussed earlier

Output

Q – The value of the internal state. 1 if the internal state is one and zero if the internal state is 0

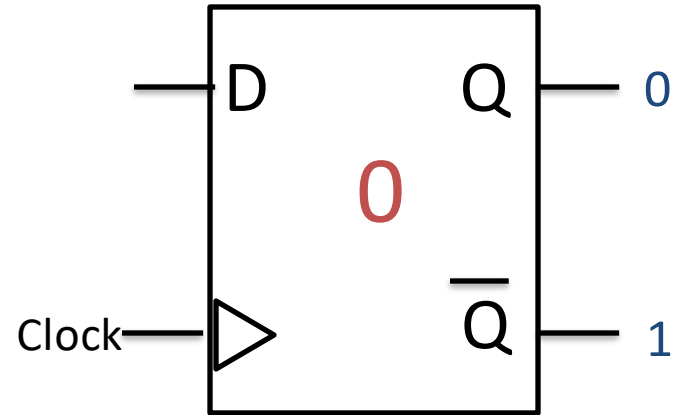
Q (bar) – Is the inverse of Q.



STATE OF A D FLIP-FLOP

Let assume that the D flip state is where its internal state is zero

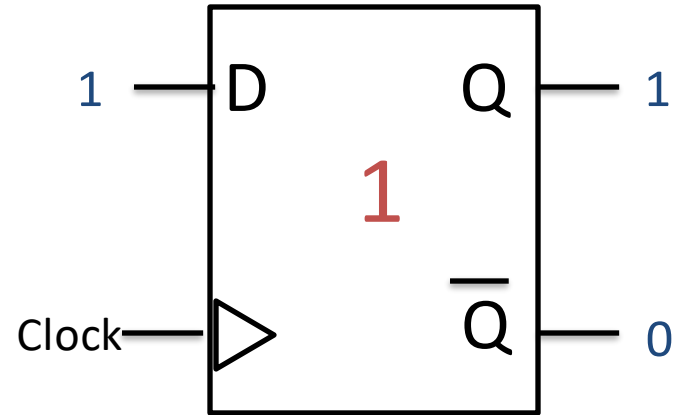
What is the value of Q and Q bar?



SETTING A D FLIP-FLOP TO 1

Now let's set the internal state of the Flip-Flop to 1 by setting D to 1

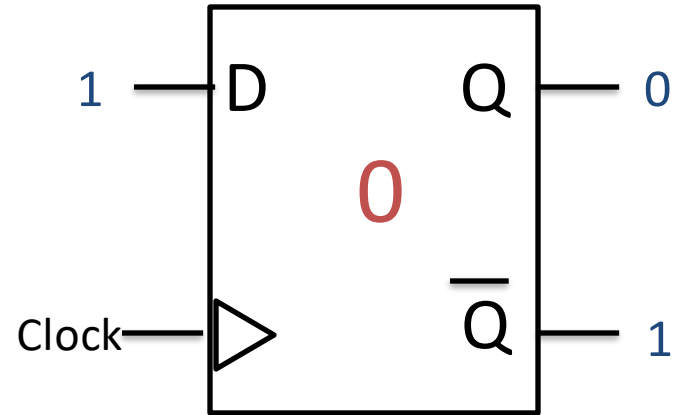
Notice that the outputs Q and Q (bar) also change.



WHAT ABOUT THE CLOCK

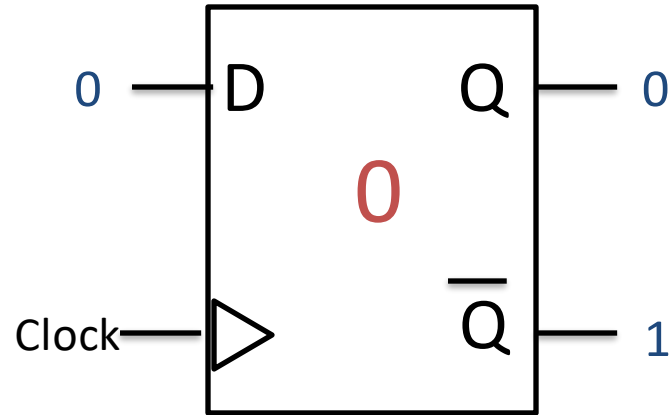
The Clock determines timing. Specifically

1. When the values change
2. How long the values remain. Let's look at an example. Where goes from 0 to 1

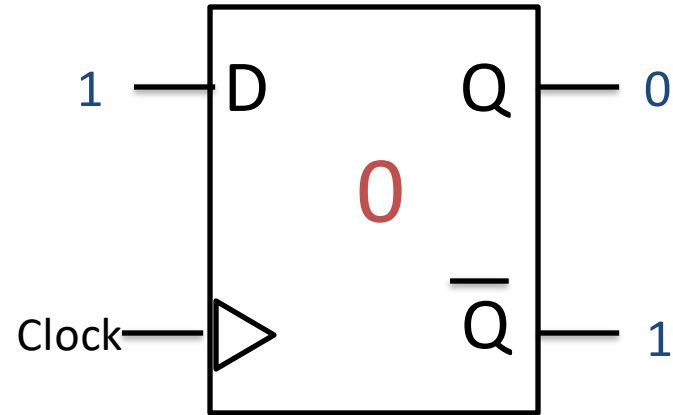
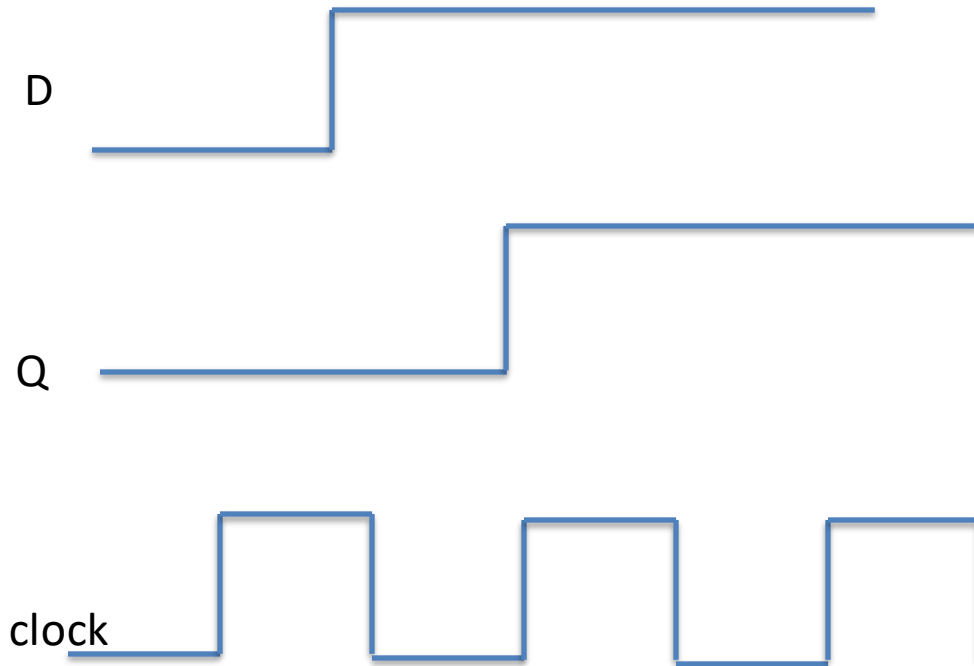


SETTING A D FLIP-FLOP TO 0

We can set the flip back to zero by setting D to **0**.
Notice that Q is now 0 and Q (bar) is now 1.

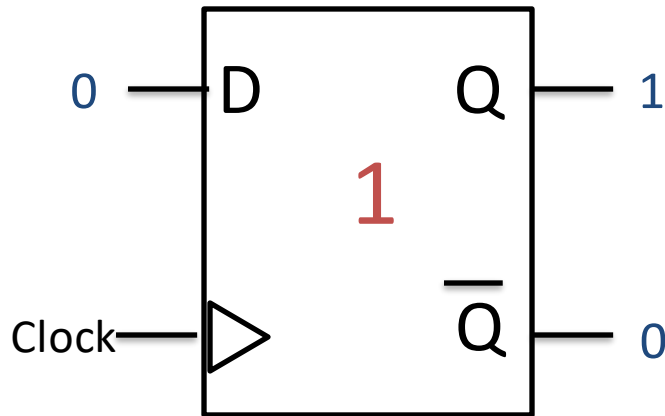
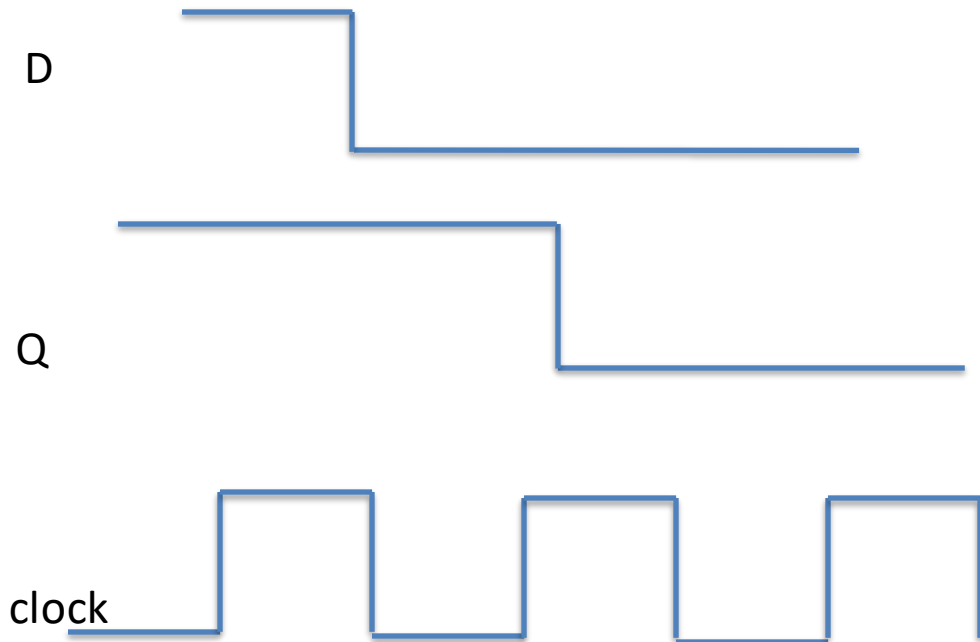


WHAT ABOUT THE CLOCK



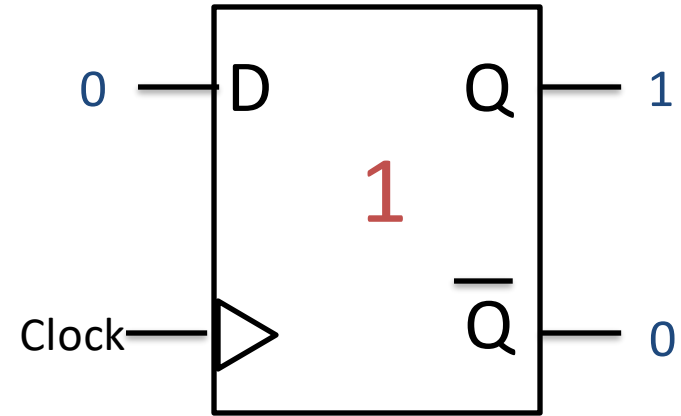
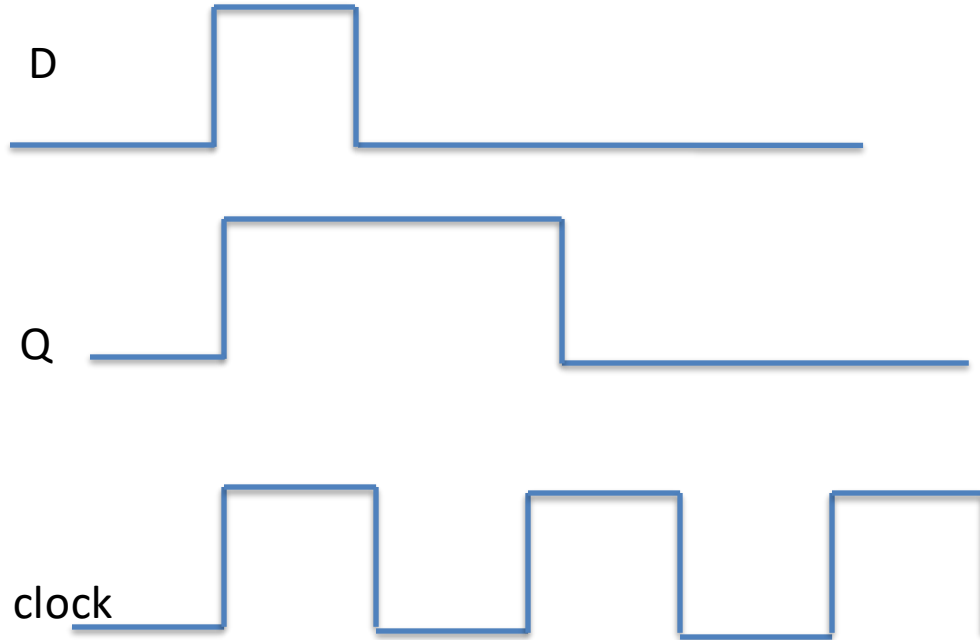
Notice that Q doesn't change until the rising edge

WHAT ABOUT THE CLOCK



Notice that Q doesn't change until the rising edge

THE FLIP FLOP HOLDS THE VALUE FOR A CLOCK CYCLE



BUILDING A REGISTER FROM FLIP FLOPS

BUILDING A REGISTER FROM FLIP FLOPS

What is a register?

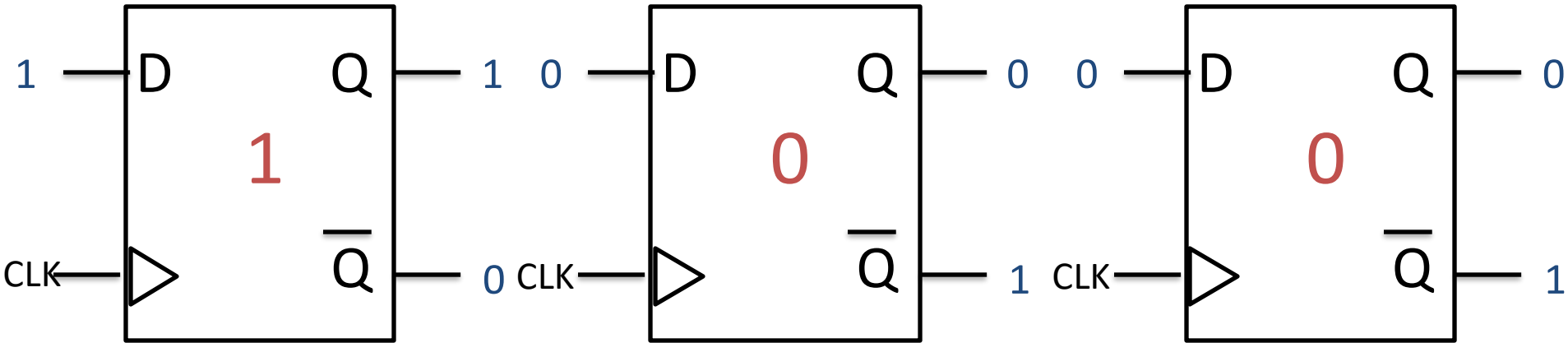
It is a memory unit that stores a bit for 1 or more or more clock cycles

Examples of things we can store in a register

The number 5 in binary 101 (This would need a three-bit register)

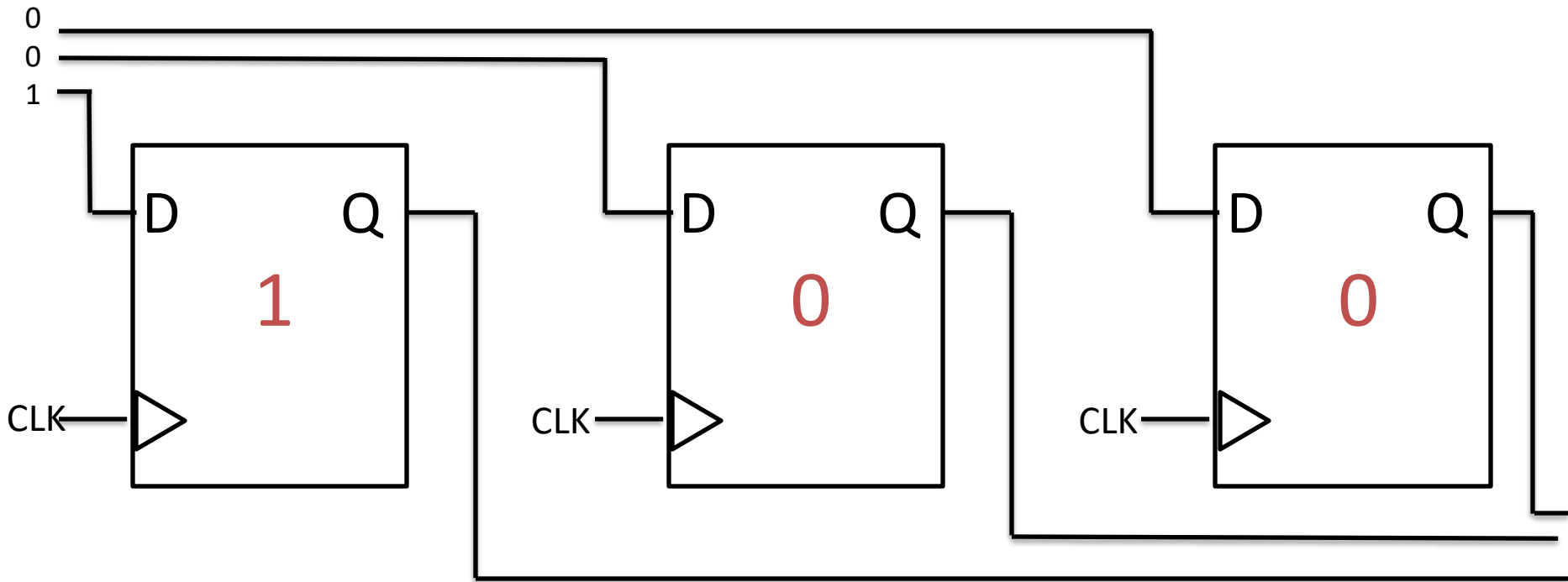
How could we build a 3-bit register?

BUILDING A REGISTER FROM FLIP FLOPS



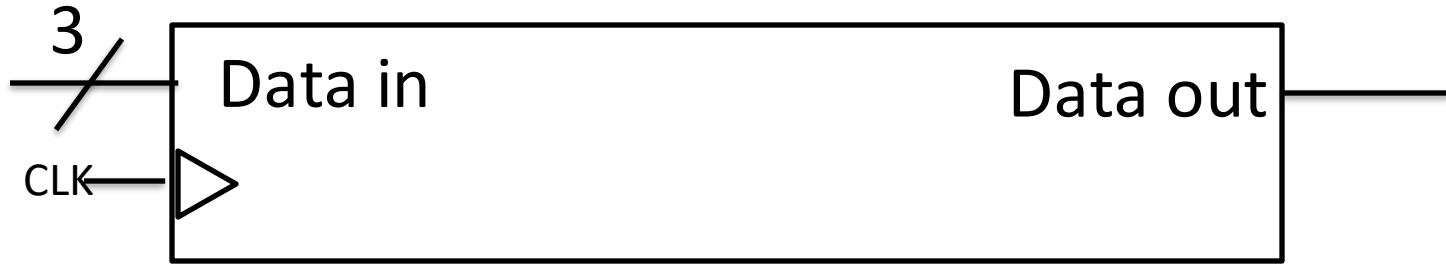
How could we build a 3-bit register? We can build a 3 bit register with three flip-flops

BUILDING A REGISTER FROM FLIP FLOPS



Removed Q (bar) for readability

REGISTER SYMBOLS

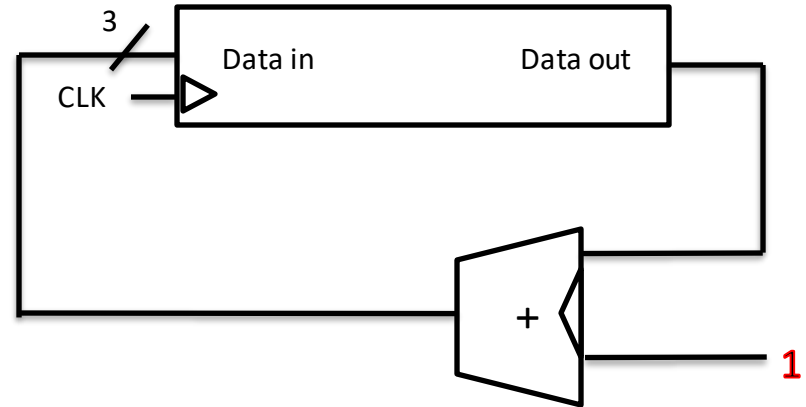


3-BIT COUNTER

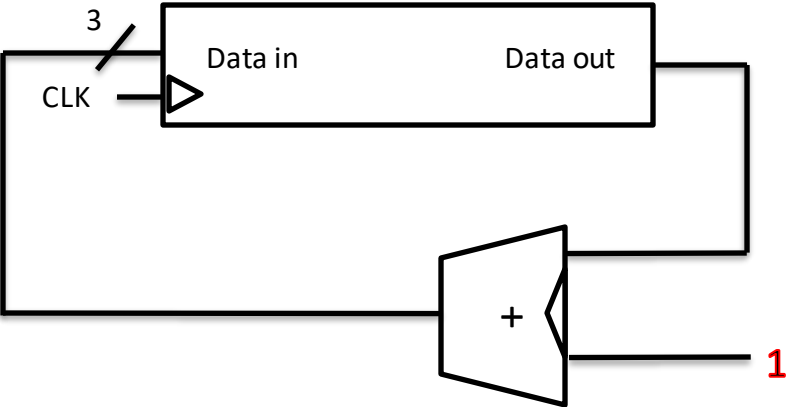
Let's put it all together and build a 3-bit counter

Circuit that counts from

000,
001,
010,
011,
100,
101,
110,
111



DRAWING 3-BIT COUNTER OVER SEVERAL CYCLES



Draw the Timing Diagram

EXAM QUESTIONS SPRING 2023

11. [4 points] The register that we discussed in class (the positive-edge-triggered D flip-flop) has inputs `D` and `clock` and output `Q`. If `Q` is 1 and the `clock` is transitioning from 1 to 0, which of the following is true? *Fill in the circle completely for all that apply.*
- `D` must also be 1 (not 0)
 - `D` may be 0 or 1
 - `Q` will transition from 1 to 0 with the clock
 - `Q` will transition to the value of `D` when the clock transitions to 0
12. [4 points] To build a 4-bit counter circuit, we could directly connect the outputs of the circuit back to the inputs without the need of a register.
- True
 - False

11. [4 points] The register that we discussed in class (the positive-edge-triggered D flip-flop) has inputs `D` and `clock` and output `Q`. If `Q` is 1 and the `clock` is transitioning from 1 to 0, which of the following is true? *Fill in the circle completely for all that apply.*
- `D` must also be 1 (not 0)
 - `D` may be 0 or 1
 - `Q` will transition from 1 to 0 with the clock
 - `Q` will transition to the value of `D` when the clock transitions to 0

B

12. [4 points] To build a 4-bit counter circuit, we could directly connect the outputs of the circuit back to the inputs without the need of a register.
- True
 - False

False

