Instructions

This exam contains 12 pages (including this cover page) and 14 questions. It is out of 100 points.

You have **50 minutes** to complete the examination. As a courtesy to your classmates, we ask that you not leave during the last 15 minutes.

For this exam, you have been given a separate answer sheet to fill in your responses.

DO shade in the bubbles on your answer sheet without going outside the lines

DO feel free to write on this exam packet

DO assume all right shift operations (>>) are arithmetic

DO NOT write anything on your answer sheet except for your name, computing ID, signature, and answers in the designated areas

DO NOT use a calculator, consult notes, or collaborate with classmates

The next page contains reference material which you are welcome to refer to during the test if you would like.

Our Example ISA

This is the same ISA used in HW03 and HW04, but presented to fit onto one printed page.

Each instruction is one or two bytes, with the meaning of those bytes being:

7	6	5	4	3	2	1	0
0	icode		a		b		

byte at pc

7	6	5	4	3	2	1	0
immediate							

byte at pc + 1

Not all instructions have the second byte; those that do describe it below as the byte "at pc + 1".

In the table below rA means "the value stored in register number a" and rB means "the value stored in register number b." All numbers are represented in two's complement.

icode	b	Behavior	add to pc
0		rA = rB	1
1		rA += rB	1
2		rA &= rB	1
3		rA = read from memory at address rB	1
4		write rA to memory at address rB	1
5	0	rA = ~rA	1
5	1	rA = -rA	1
5	2	rA = !rA	1
5	3	rA = pc	1
6	0	rA = read from memory at pc + 1	2
6	1	rA += read from memory at pc + 1	2
6	2	rA &= read from memory at pc + 1	2
6	3	rA = read from memory at the address stored at pc + 1	2
7		if rA <= 0, set pc = rB	N/A
7		if rA > 0, do nothing	1

1 Bitwise Operations

1. (6 points) In 16-bit two's complement, what is the result of the following operations? Give your answers in hexadecimal.

   A. `0xABED << 8`

   B. `(0xABED >> 8) << 4`

   Solution:

   A. `0xED00`

   B. `0xFAB0`

2. (3 points) Complete the function below so that it sets the n-th bit of an integer `x` to `1`, where the leftmost bit of `x` is bit `0`.

   ```
   def set_nth_bit(x, n):
       return x | (1 << ____)
   ```

   Solution:

   The question should have read that the *rightmost* bit of `x` is bit `0`. Answers conforming to either the written or intended interpretation receive full credit.

   If the leftmost bit of `x` is bit `0` as written, the following are plausible correct answers:

   - `7 - n` (assuming `x` is an 8-bit integer)
   - `15 - n` (assuming `x` is a 16-bit integer)
   - `31 - n` (assuming `x` is a 32-bit integer)
   - `63 - n` (assuming `x` is a 64-bit integer)

   If the rightmost bit of `x` is bit `0` as intended, the correct answer is `n`.

3. (4 points) Complete the function below so that it swaps odd and even bits in a 32-bit integer `x` (e.g., `1010` becomes `0101`).

   ```
   def swap_odd_even_bits(x):
       odd_bits = x & 0xAAAAAAAA  # Mask for odd bits
       even_bits = x & 0x55555555  # Mask for even bits
       return (odd_bits >> A.____) | (even_bits << B.____)
   ```

Solution:

    A. `1`

    B. `1`

4. (6 points) Consider the pseudocode below:

```
parity = 0
repeat 32 times:
    parity = parity  1  (x  2  1)
    x = x  3  1
```

If `parity` is to give the (even) parity of the 32-bit number `x` after this code runs, which bitwise operator should be substituted for

    A. Box 1

    B. Box 2

    C. Box 3

Solution:

    A. XOR or `^`

    B. AND or `&`

    C. Right shift or `>>`

2   Number Representation

5. (12 points) Assuming an 8-bit two's complement number representation, complete the following table with the correct representations:

Binary	Decimal	Hexadecimal
	101	
0b11111111		
		0x86

Solution:

Row 1: 0b01100101, 0x65

Row 2: -1, 0xFF

Row 3: 0b10000110, -122

6. (5 points) Consider the following 8-bit IEEE-style floating-point number with a 3-bit exponent:

    `11011010`

Write it in decimal.

Solution: -6.5

7. (4 points) The hexadecimal number `0x2240` is to be stored in 2 bytes of memory starting at address `0x0010`. What byte will be stored at address `0x0011` if the number is stored in

   A. Big-Endian?
   B. Little-Endian?

Solution:

   A. 0x40

   B. 0x22

8. (6 points) Translate the 8-bit binary number `0b11001101` to decimal assuming its number representation is

   A. Unsigned
   B. Signed using sign bit
   C. Signed using a bias of 127
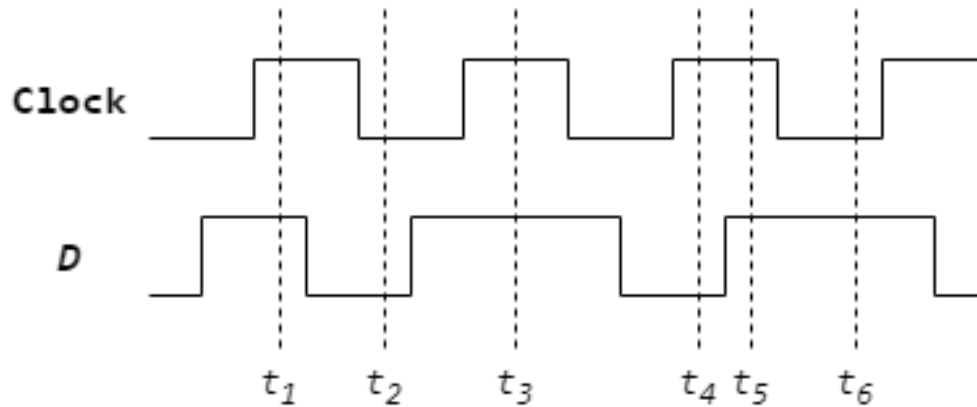
Solution:

A. 205

B. -77

C. 78

3   Logic Gates and Circuits

9. (10 points) The timing diagram below shows the clock and input (D) signals for a positive edge-triggered D-flip-flop. Complete the table with the corresponding output Q.

Time	t_1	t_2	t_3	t_4	t_5	t_6
Q	1					

Solution:

t_2: 1

t_3: 1

t_4: 0

t_5: 0

t_6: 0

10. (8 points) How many select bits (or lines) are needed to assign an input to the output for each of the following mux configurations?

    A. 4-1 mux with 4-bit inputs

    B. 4-1 mux with 8-bit inputs

    C. 8-1 mux with 4-bit inputs

    D. 8-1 mux with 8-bit inputs

Solution:

   A. 2
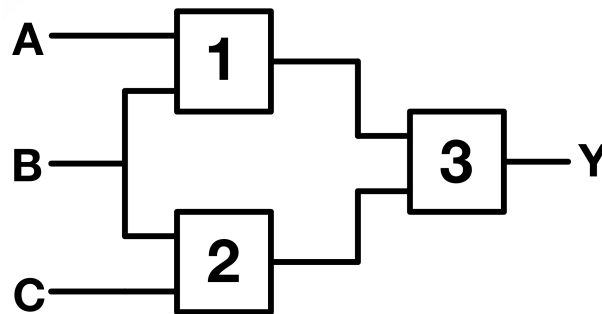
   B. 2

C. 3

D. 3

11. (6 points) Implement the following logic expression by specifying which logic gate should go in each box. Here, · represents the AND operation, ⁻ represents NOT, and + represents OR.

$$Y = \overline{(A \cdot B)} + (B \cdot C)$$

A. Box 1 (Write AND, OR, NOT, NAND, etc in the provided box)
B. Box 2 (Write AND, OR, NOT, NAND, etc in the provided box)
C. Box 3 (Write AND, OR, NOT, NAND, etc in the provided box)
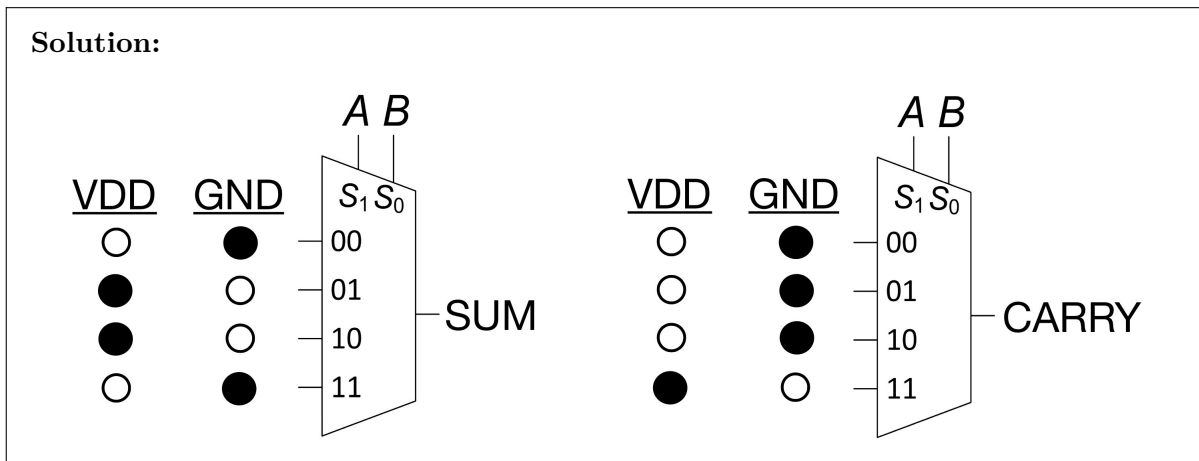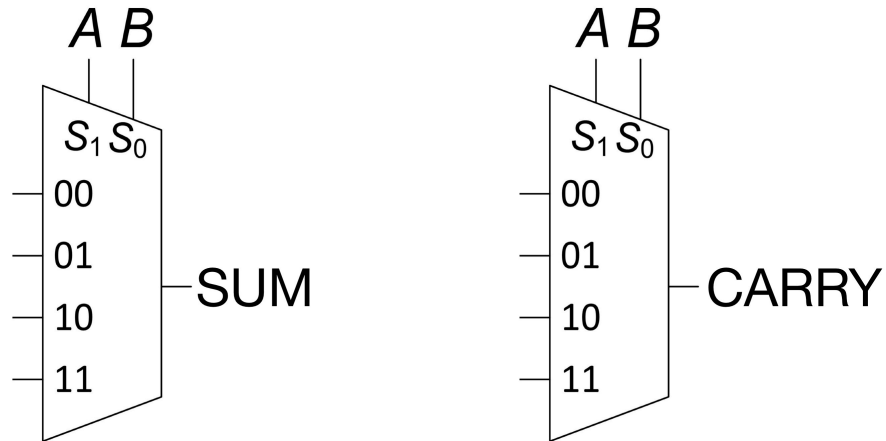
Solution:

A. NAND

B. AND

C. OR

12. (8 points) Consider the Boolean expressions that implement a half adder, where $\cdot$ represents the AND operation, and $\oplus$ represents XOR.
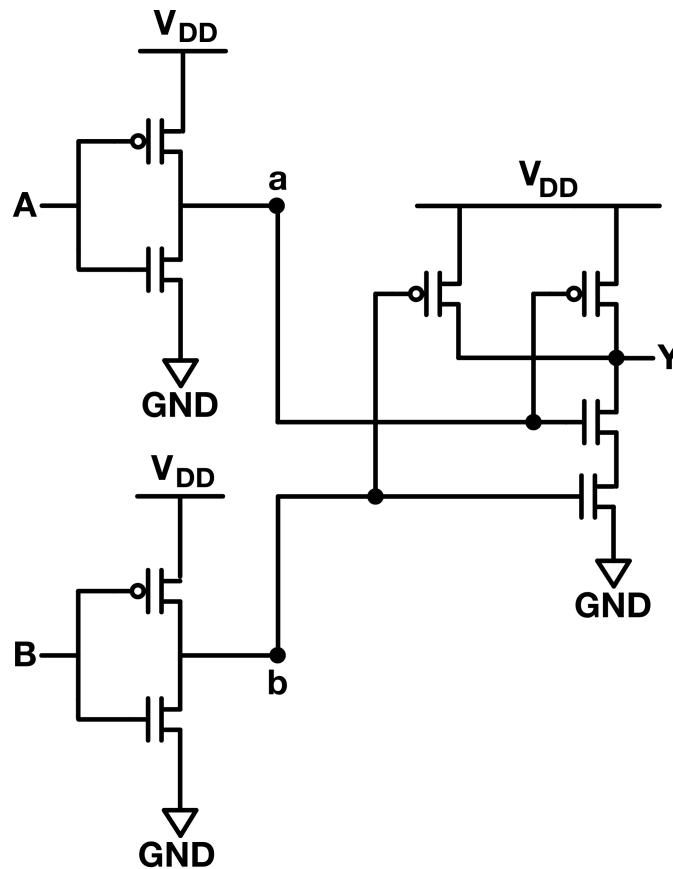
$$SUM = A \oplus B$$

$$CARRY = A \cdot B$$

Implement a half adder using only two 4-1 muxes by fixing each input to either VDD or GND.

Solution:

13. (7 points) Consider the following CMOS logic circuit in which A and B are inputs and Y is the output:

A. Which two CMOS logic gates can be used to construct this circuit?

B. Complete the following truth table with the corresponding values.

A	B	a	b	Y
0	0			
0	1			
1	0			
1	1			

C. Which logic gate does this circuit implement?

Solution:

  A. NOT and NAND

B. a: 1, 1, 0, 0 b: 1, 0, 1, 0 Y: 0, 1, 1, 1

C. OR

4   Toy ISA

14. (15 points) The following tables present the current state of a Toy ISA Machine.

Register	Value
r0	0x12
r1	0x34
r2	0xAB
r3	0xCD
pc	0x09

Table 14.1: Register values

Memory Address	...	0xFB	0xFC	0xFD	0xFE	0xFF
Value	...	0xCA	0xA1	0x13	0x36	0xF7

Table 14.2: Selection of memory values

For each sequence of hexadecimal Toy ISA instructions listed below, give the hexadecimal values of the indicated registers or memory locations after the instructions are executed.

You may assume the Toy ISA Machine has the initial state described above for all questions.

A. `0x55 0x74`

   r0: **0x12**   r1: **0xCC**   pc: **0x12**

B. `0x67 0xFE`

   r1: **0x36**   M[0xFE]: **0x36**   pc: **0x0B**

C. `0x58 0x06`

   r0: **0x12**   r1: **0x54**   r2: **0x54**

D. `0x6E 0xFB`

   r2: **0xAB**   r3: **0xC9**   M[0xFB]: **0xCA**

E. `0x60 0xFF 0x48`

   r0: **0xFF**   r2: **0xAB**   M[0xFF]: **0xAB**